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RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2811

PATENT APPLICATION
Docket. No. 9898-208
Client No. SS-15400-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Ki-Won Choi	Confirmation No.	6747
Serial No.	10/055,266	Examiner:	Quang D. Vu
Filed:	January 22, 2002	Group Art Unit:	2811
For:	SEMICONDUCTOR PACKAGE HAVING CHANGED SUBSTRATE DESIGN USING SPECIAL WIRE BONDING		

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR 1.116

Responsive to the Final Office Action, Paper No. 6, dated July 11, 2003, please amend the application as follows.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop AF; Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450
Date: November 10, 2003

Adrienne Chocholak

IN THE CLAIMS

1. (Previously presented) A semiconductor package comprising:

a substrate including a redundant bond finger, an added bond finger connected to a redundant solder ball pad;

a semiconductor chip having an added bond pad attached to the substrate;

a normal wire bonding unit coupled between the added bond pad and the redundant bond finger; and

an added wire bonding unit coupled between the redundant bond finger and the added bond finger,

wherein the added bond pad is electrically connected to the redundant solder ball pad via the redundant bond finger and the added bond finger.

2. (Original) The semiconductor package of claim 1, further comprising:

an encapsulant for encapsulating the semiconductor chip, the normal and added wire bonding units.

3. (Original) The semiconductor package of claim 2, further comprising:

a solder ball connected to the redundant solder ball pad.

4. (Original) The semiconductor package of claim 1, wherein the substrate is a single-layer substrate on which a printed circuit pattern is formed.

5. (Original) The semiconductor package of claim 1, wherein the substrate is a double-layer substrate or a multi-layer substrate.

6. (Original) The semiconductor package of claim 1, wherein a solder mask is not formed on the added bond finger.

7. (Original) The semiconductor package of claim 1, wherein the added wire bonding unit is formed over the substrate.

8. (Original) The semiconductor package of claim 1, wherein the added wire bonding unit is formed on an outer region of the substrate on which the semiconductor chip is mounted.

9. (Original) The semiconductor package of claim 1, wherein the added wire bonding unit is one unit or a plurality of units.

10. (Original) The semiconductor package of claim 1, wherein the semiconductor chip is attached to the substrate using an adhesive.

11. (Cancelled)

12. (Original) The semiconductor package of claim 1, wherein the added bond finger has the same pad shape as that of the redundant bond finger.

13. (Previously presented) A semiconductor package comprising:

a substrate including a first printed circuit pattern connected to a redundant bond finger and a second printed circuit pattern connected to a redundant solder ball pad;

a semiconductor chip attached to the substrate; and

an added wire bonding unit coupled between the first printed circuit pattern to the second printed circuit pattern to electrically connect the redundant bond finger to the redundant solder ball pad.

14. (Original) The semiconductor package of claim 13, further comprising:

an encapsulant for encapsulating the semiconductor chip and the added wire bonding unit.

15. (Original) The semiconductor package of claim 14, further comprising:

a solder ball connected to the redundant solder ball pad.

16. (Original) The semiconductor package of claim 13, wherein the first and second printed circuit patterns each have a width that enables wire bonding to be performed thereon.

17-25 Cancelled)

26. (Previously presented) A semiconductor package comprising:

a semiconductor chip having an added bond pad;

a substrate having a redundant bond finger and an added bond finger connected to a redundant solder ball pad;

a normal wire bonding unit coupled between the added bond pad and the redundant bond finger; and

an added wire bonding unit coupled between the redundant bond finger and the added bond finger such that the added bond pad is electrically connected to the redundant solder ball pad via the redundant bond finger and the added bond finger.

27. (Currently amended) The semiconductor package of claim ~~17~~, 26 wherein the added bond finger is not directly connected to the added bond pad

REMARKS

Claims 1-10, 12-16, 26 and 27 are pending.

Claims 1-10, 12-16, 26 and 27 are rejected.

Claim 27 is objected to.

Claims 1, 3-4, 6-10, 16, 26 and 27 are rejected under 35 U.S.C. 102(e).

Claims 2, 5, 12 and 14 are rejected under 35 U.S.C. 103(a).

Claim 27 is amended to properly depend on claim 26.

No new matter is added.

Claims 1-10, 12-16, 26 and 27 remain in the case for consideration.

Applicant request reconsideration and allowance of the claims in light of the above amendment and following remarks.

Specification

The disclosure stands objected to. The Examiner has argued that the phrase of lines 10-12, page 6 of the present application, i.e., "the substrate is a single layer, a double layer, or a multi layer substrate" is unclear. The Examiner has further stated that "Figure 6 shows that the substrate (100) includes the substrate and printed circuit pattern (106)" and asked whether the substrate is referred to a single layer or a double layer substrate.

The phrase at page 6, lines 9-11 of the instant application simply states that "Thus, the semiconductor package can be manufactured without adding a micro-via hole to the substrate 100 *regardless of* whether the substrate 100 is a single-layer substrate, a double-layer substrate, or a multi-layer substrate." (Emphasis added)

One skilled in art, therefore, will understand that the substrate 100 can be any one of a single-layer substrate, a double-layer substrate, or a multi-layer substrate, as in known in the art. In the present invention, because the semiconductor package can be manufactured without adding a micro-via hole to the substrate 100 *regardless of* whether the substrate 100 is a single-layer substrate, a double-layer substrate, or a multi-layer substrate, a small-sized semiconductor package can be realized, and the cost to change the design of the substrate can be reduced.

For these reasons, the specification is not unclear and, therefore, Applicant respectfully requests that the objection to the specification be removed.

Claim Objections

Claim 27 is objected to. Claim 27 is now amended to properly depend on claim 26. Applicant requests that the claim objection be removed.

Claim Rejections – 35 USC § 102

Claims 1, 3-4, 6-10, 16, 26 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,448,664 to Tay et al., ("Tay").

The rejections are respectfully traversed.

The Examiner has argued that Tay teaches, among other things, "an added wire bonding unit (a line connecting [76] and the added bond bond finger) coupled between the redundant bond finger (76) and the added bond finger (a pad formed along the first inner rectangle)."

Tay does not, however, teach such an added wire bonding unit coupled between the redundant bonder finger and the added bond finger.

Tay is merely directed to providing BGA chip packages that can be easily burned-in and tested by existing test tooling, e.g., with test pads arranged in a conventional TSOP pin-out pattern to allow for the use of existing test apparatus and test tooling, in order to minimize the lead time and associated costs for introducing BGA chip packages. See col. 5, lines 43-45; col. 6, lines 33-38; and col. 11, lines 27-34 of Tay.

In particular, in Tay, bond wires 108 are merely coupled between die bond pads 106 and substrate bond pads 76 (See, for example, FIG. 9B and col. 10, lines 1-7), which are, in turn, placed in electrical communication with selective solder balls 80 by circuit traces 78. Then, the selected solder balls 80 are placed in electrical communication with test contact pads 84 through second circuit traces 82 so as to provide a conductive path from the test contact pad 84 back to at least one selected substrate bond pad 76. See col. 9, lines 35-44 and FIG. 6 of Tay. (Please note that completed chip package 88 in FIG. 9 of Tay has been shown as being trimmed so as to remove test contact pads 84 from the chip package 88. See col. 11, lines 12-26 of Tay.)

With this arrangement of Tay, semicompleted chip package can then be placed in a conventional burn-in and test apparatus which includes test tooling. In particular, test contact pads located on the periphery of substrate with complimentarily positioned probes that are preferably arranged in the same TSOP pin-out configuration as the underlying test contact pads 84. That is, there is a corresponding probe 102 for each test contact pad to a respective

substrate bond pad 76, which, in turn, is in electrical communication with a respective die bond pad 106 by way of a bond wire 108. See col. 10, lines 43-68 of Tay.

Therefore, in Tay, there is absolutely no need for an added wire bonding unit coupled between the redundant bonder finger and the added bond finger, other than the electrical connections described above, unlike the claimed invention.

In contrast, in the claimed invention, by utilizing the added wire bonding unit 114, the substrate 100 can still be used without changing the package substrate design, even if semiconductor chip design is changed slightly. See page 6, lines 3-8 of the present application. Thus, with the claimed invention, the semiconductor package can be manufactured without adding a micro-via hole to the substrate 100 regardless of whether the substrate 100 is a single-layer substrate, a double-layer substrate, or a multi-layer substrate. See page 6, lines 9-12 of the present application.

For these reasons, nowhere does Tay teach or disclose such aspects and needs of the present invention.

Therefore, Tay does not teach all of the limitations of claim 1, for example, "an added wire bonding unit coupled between the redundant bond finger and the added bond finger, wherein the added bond pad is electrically connected to the redundant solder ball pad via the redundant bond finger and the added bond finger."

Consequently, Tay does not anticipate claim 1 and claim 1 is allowable. Also, claims 2-10 and 12, which depend from allowable claim 1 and recite features that are neither taught nor disclosed in the cited references, are also allowable.

With respect to claim 13, for the reasons discussed above, Tay does not teach or disclose, "an added wire bonding unit coupled between the first printed circuit pattern to the second printed circuit pattern to electrically connect the redundant bond finger to the redundant solder ball pad," as recited in claim 13. Therefore, claim 13 is allowable and claims 14-16, which depend therefrom, are also allowable for their own merits and their dependency.

In addition, for the reasons discussed above, claim 26, which recites limitations similar to claim 1, is allowable and claim 27, which depends from claim 26, is also allowable for its own merits and its dependency.

Claim Rejections – 35 USC § 103

Claims 2, 5, 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tay in view of the Admitted Prior Art.

The rejections are respectfully traversed.

As discussed above, Tay does not teach or disclose, for example, "an added wire bonding unit coupled between the redundant bond finger and the added bond finger, wherein the added bond pad is electrically connected to the redundant solder ball pad via the redundant bond finger and the added bond finger."

Thus, the cited references, either alone or in combination, do not teach or suggest all of the limitations of claims 2, 5, 12 and 14. Accordingly, the rejection does not present a *prima facie* case of obviousness. Therefore, claims 2, 5, 12 and 14 are allowable.

In Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-10, 12-16, 26 and 27 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Alan T. McCollom
Reg. No. 28,881

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
503-222-3613